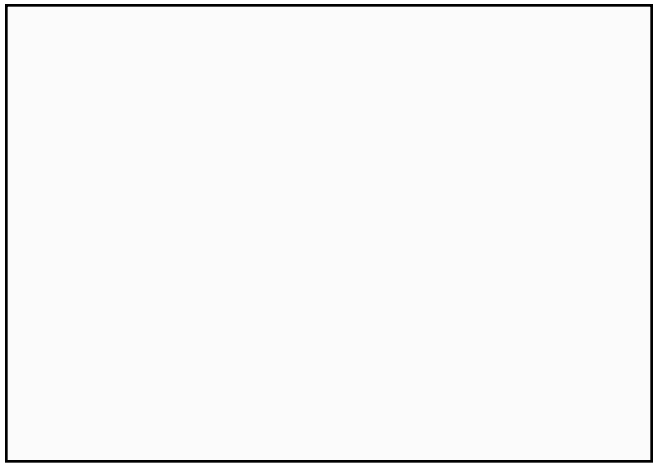

# *CSC Integration*

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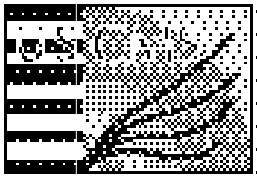
# Chronology

## 06 Oct 99

- P2'' returned to FNAL

## 07 Oct 99 - present

- Chamber commissioning
- DAQ setup
- Noise studies
- Threshold studies
- 16-channel anode board commissioning
  - Can be stacked 3 high for ME1/3 solution
- LV DC-DC converter tests
- ALCT integration model



# LV Supplies

**Initial setup used linear supplies**

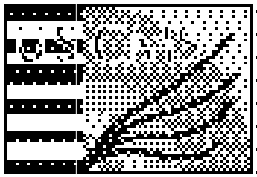
**Then brought up Vicor DC-DC converters**

- **Found some problems in the distribution strips**
- **Filter circuit modified**
- **Vicor noise invisible to CFEBS, can be seen on anodes**

**LV distribution design has been worked out**

**Radiation resistance of Vicors & RAM filters needs to be evaluated**

- **Early model of Vicor DC-DC converters failed at low dose rates (H. Takai, BNL)**
  - Element that failed was optocouper
  - Design changed to use magnetic feedback
- **We will test samples of 2nd-generation units at PROSPERO facility in December**



# HV Issues

## HV connectors

- **Caton connectors**
  - Connectors on cable end can spark at 5kV
  - Sockets on cable end too close to surface of insulator
- **Caton is modifying connector design**

## HV cables

- **Leakage in cable assemblies**
  - Identified as leakage through the cable dielectric itself
  - Insulation thickness spec for cable has been modified
- **May want to go to individual wires for internal HV wiring**
  - Ordered two connectors with “octopus” leads to test this scheme for P4
- **Will want to move third HV connector to provide path for signal cables**

# CSC Side Panel Screws

**P2'' came back from CERN with several side panel screw holes stripped**

**Evaluated hardness of frame extrusions**

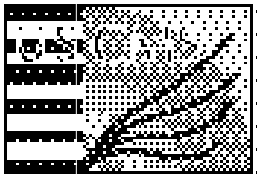
- **Believe that at least one of the rails is below spec**

**Evaluated alternative fastener designs**

- **Thread-forming screw -> conventional bolt**
- **Tapped hole, conventional bolt**
- **Threaded inserts**
- **Threaded studs**

**Thread-forming screws were superior to all economical alternatives**

**Set torque limit specs for initial seating, reinstallation of screws**



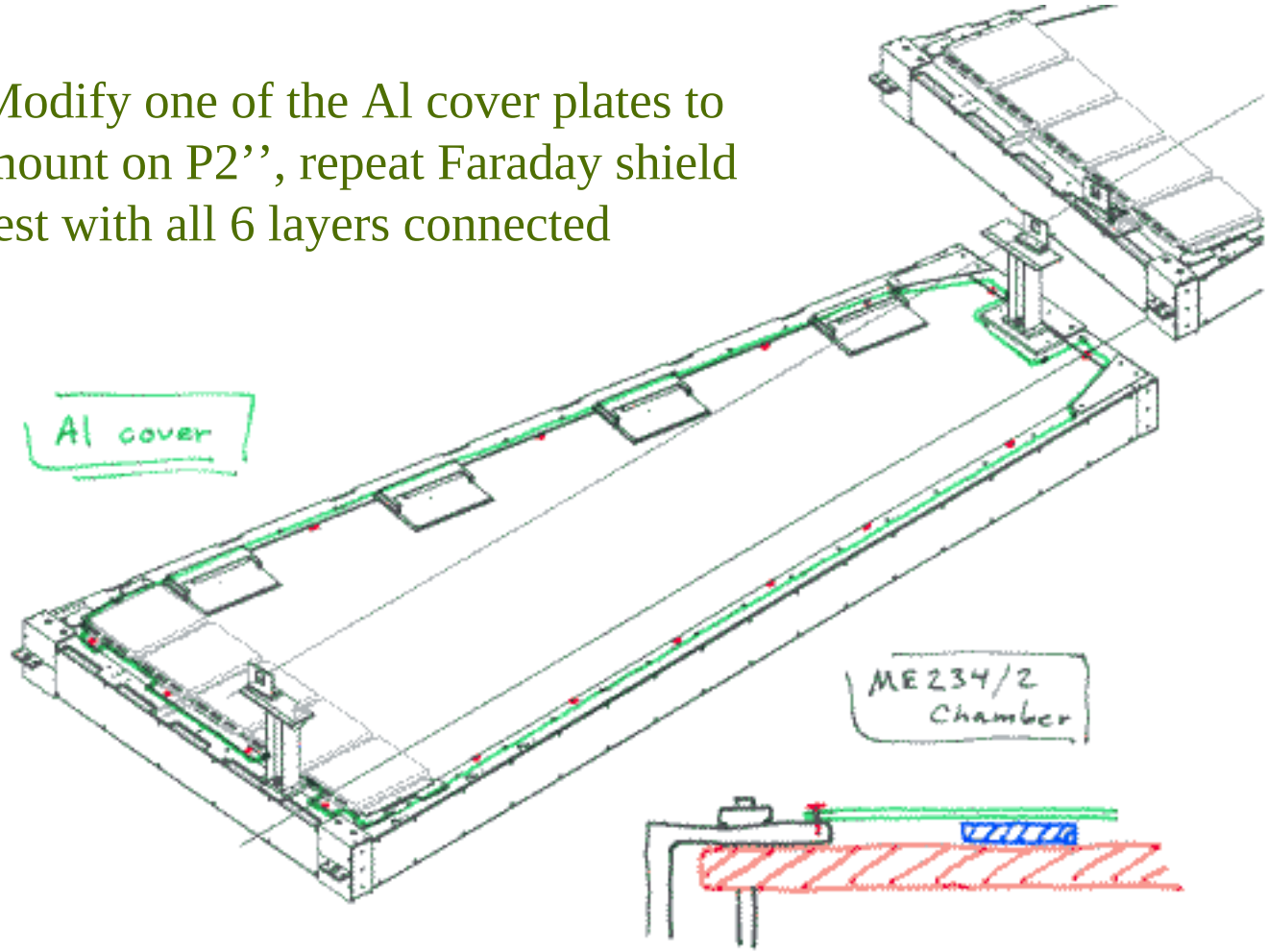
# Alignment

## From integration point of view ...

- **Radiation issues**
  - On-board switching supplies are weak link
  - Can we use 3.3v directly?
- **Cable noise**
  - I/O circuit changed to use LVDS transcievers
  - Could go to shielded Cat.5 cable
  - Will test radiated noise at Lab 7
- **Interference with cathode cables**
  - Round shielded cable is baseline solution, will test
  - Could use flat cable, but this would require rerouting of cathode board
  - Flat cable may have advantages

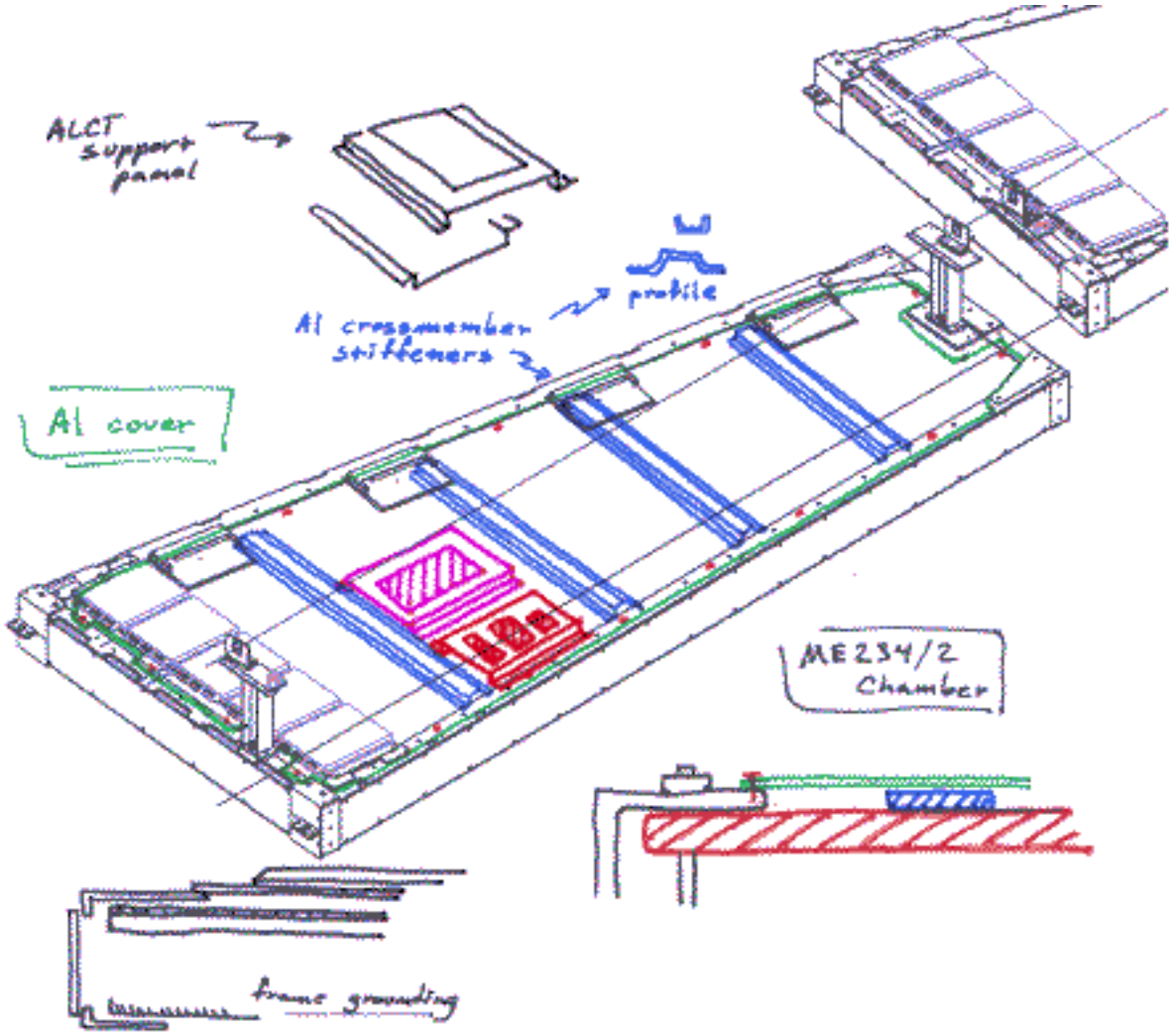
# Al Faraday shield test

Modify one of the Al cover plates to mount on P2’’, repeat Faraday shield test with all 6 layers connected

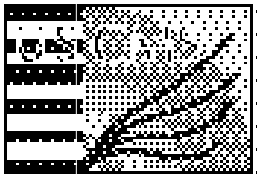


# Top shield integration

Al Cover will also provide mounting surface for on-chamber services




Stiffener ribs needed to prevent cover from bowing out once chamber is turned vertically



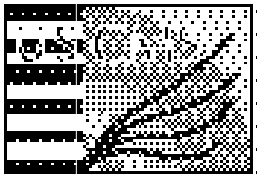
# Schedule

## Nov. 99

- Install Al cover plate
- Restore cooling system
- Finish noise tests

## Dec. 99

- Anode cabling
- CFEB cabling
- Finalize grounding scheme
- Prototype covers for anode cables
- Prototype of on-chamber mechanical parts
- Resolve HV connector issues
- Model for cable routing



# Topics that need attention ...

**Proliferation of LV supply voltages**

**Cooling system**

- integration with CFEB and ALCT design groups

**Coordination with ME1/1 group**

**ALCT input time alignment**

- Test strip / ALCT input? Both?
- Who will evaluate the problem?
- What needs to be done at integration level?

**CFEB overvoltage tests**